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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,940	01/16/2004	David William Boerstler	AUS920030715US1	8206

7590 07/27/2005

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,940	BOERSTLER ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 20 June 2005.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 06/20/05. A new ground of rejection is introduced as necessitated by amendment.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "two paired transistors in parallel" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 27 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The original specification fails to teach "two paired transistors in parallel".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya et al. (USP 4748352) in view of Alvarez (Fundamental Ckcuit Analysis, printed by Science Research Associates, Inc, 1978, pages 378-379) (previously cited).

Kamiya et al.'s figure 6 shows a method for current leakage correction for a leaky capacitor (C2), wherein the leaky capacitor is connected to ground, comprising: measuring voltage across the leaky capacitor (by 15); providing the measured voltage to a second capacitor (C3), and providing a sustaining charge (by 11) to the leaky capacitor. Thus, figure 6 shows all limitations of the claim except for a scaled capacitor that is smaller than the leaky capacitor. However, Alvarez teaches in pages 378-379 that a capacitor can be made by a plurality of parallel connected capacitors having different sizes in order to meet a desire capacitance.

Therefore, it would have been obvious to one having ordinary skill in the art to use plurality of parallel connected capacitors having different sizes for Kamiya et al.'s capacitor C3 due to doctrine equivalent function and in order to meet a particular desire capacitance of capacitor C3. Thus, the smallest capacitor in the plurality of parallel capacitor is considered as a scaled capacitor, and the scaled capacitor has an area reduced by a scaling factor in comparison to the leaky capacitor.

6. Claims 1, 2, 7, 13, 15-17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya et al. (USP 4748352) in view of Alvarez (Fundamental Ckcuit Analysis, printed by Science Research Associates, lnc, 1978, pages 378-379) (previously cited) and Stokstad (USP 6121764).

As to claims 1 and 16, the combination of Kamiya et al. add Alvarez references fails to show the detail of the current source 11. However, Stockstad's figure 1 shows a current source having high output impedance, thereby provides accurate output current. Therefore, it would have been obvious to one having ordinary skill in te art to use Stokstad's current source for Kamiya et al.'s current source 11 for the purpose of generating an accurate desired current. Thus, the modified Kamiya et al.'s figure 6 shows an apparatus for current leakage correction coupled to a leaky capacitor (Kamiya et al.'s capacitor C2), the leaky capacitor is connected to ground, comprising: a scaled capacitor (the smallest capacitor in the modified capacitor C3), wherein the scaled capacitor has an area reduced by a scaling factor in comparison to the leaky capacitor; and a plurality of current mirrors (the modified current source 11 and CM2), wherein the plurality of current mirrors further comprise: at least one first current mirror (the modified 11) is at least configured to be coupled to the leaky capacitor; and at least one second current

mirror (CM2) is at least configured to be coupled to the scaled capacitor that is at least configured to provide a potential difference across the scaled capacitor that is substantially equal to a potential difference across the leaky capacitor minus the potential difference across the at least one second current mirror.

As to claims 2 and 17, the modified Kamiya et al.'s figure 6 shows that the plurality of current mirror further comprises a plurality of transistors.

As to claims 7 and 22, the modified Kamiya et al.'s figure 6 shows that the plurality of current mirrors further comprise a plurality of bipolar transistors.

As to claims 13 and 15, the modified Kamiya et al.'s figure 6 shows that the step of providing the measured voltage to a scaled capacitor further comprises utilizing a plurality of current mirrors (11 and CM2) with an adjusted width and length to provide the measured voltage to the scaled capacitor.

7. Claims 3-6, 8-11, 18-21 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya et al. (USP 4748352) in view of Alvarez (Fundamental Ckcuit Analysis, printed by Science Research Associates, lnc, 1978, pages 378-379) (previously cited) and Stokstad (USP 6121764) and Otake (USP 5689178).

As to claims 3, 8, 18 and 23, the modified Kamiya et al.'s figure 6 fails to shows that the transistor are FETs. However, Otake teaches in Col.2, lines 15-20, that MOSFET is faster than bipolar transistor. Therefore, it would have been obvious to one having ordinary skill in the art to use MOSFETs for transistors in Kamiya et al.'s figure 6 for the purpose of improving the speed of circuit.

As to claims 4, 9, 19 and 24, the modified Kamiya et al.'s figure 6 shows that at least one MOSFET (MOSFETs in 11) of the plurality of MOSFETS is a Positive-channel FET (P-MOSFET), wherein the P-MOSFET is at least configured to inject current into the leaky capacitor to compensate for a current leak.

As to claims 5, 6, 10, 11, 20, 21, 25 and 26, the modified Kamiya et al.'s figure 6 that at least one MOSFET of the plurality of MOSFETS is a Negative-channel FET (N-MOSFET) (MOSFETs in CM2).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
Art Unit 2816

July 25, 2005